hardware complexity and/or software processing load and complexity compared to the existing algorithm

I.4.2 Enhanced Bit and Confidence Declaration

I.4.2.1 Overview

The current technique of declaring a bit based upon the higher of the two chips will generate bit errors in cases of higher level overlapping Mode A/C fruit (Figure I-2, part c). The use of amplitude to correlate the received pulse with the preamble pulse level will improve bit declaration accuracy. Four techniques have been investigated. One is a very simple approach that uses only the amplitude measured at the center of each chip. The remaining three ~~follow~~ use a ~~somewhat~~ more ~~complex~~ capable approach that takes advantage of the four samples per chip that are taken in the current technique to establish bit confidence. Each of these techniques is described in the following paragraphs.

The following description of the center sample technique is ~~included only~~intended to provide an example of processing performance needed to meet the requirements of Class A1 equipment. This description also serves as an introduction to the ~~two~~ three more ~~complex~~ capable approaches. The center sample technique will not provide sufficient performance to meet requirements specified for Class A2 and A3 equipment in the test procedures of §2.4.4.4. The specified performance for these latter classes of equipment can only be meet by an approach that performs equivalently to one of the multi-sample techniques.

I.4.2.2 Use of Center Amplitude

An improvement in the declaration of Mode S data bits can be achieved if the actual amplitudes of the center samples of the '1' and '0' chips can be measured for each data position, rather than just a comparison of which chip sample is greater. All Mode S pulses, including those of the preamble, have approximately the same level (within 1 or 2 dB). Thus if the preamble level is measured, the expected level of each data pulse will be known. Then if both center samples of a data position are above threshold, but only one is within a ±3 dB band centered at the preamble level, it would be reasonable to assume that the corresponding chip is the correct Mode S pulse location. This is illustrated in Figure I-2, part d.

Figure I-3 illustrates the new data and confidence declaration algorithms that result when the actual sample amplitudes can be measured, and both samples are above threshold. As shown in Figure I-3, a bit is high confidence when 1 and only 1 of the two samples correlate with the preamble level. The correlating sample, rather than the larger sample, is declared to be the true data value. If both samples, or neither sample, correlates with the preamble, a low confidence bit is declared. In this case, the larger sample is selected as the bit value, as in the current technique.